

In the Claims:

1. (Currently amended) An integrated circuit memory device, comprising:
first and second memory blocks; and
a sense amplifier array [[that is]] extending between and electrically coupled to said first and second memory blocks by first and second pluralities of pairs of bit lines, respectively, said sense amplifier array having first and second column select I/O blocks therein [[that are]] arranged in an alternating zig-zag layout sequence that extends between immediately opposing sides of said first and second memory blocks.
2. (Currently amended) The memory device of Claim 1, wherein said sense amplifier array has first and second rows therein that are immediately adjacent to each other; and wherein the first and second column select I/O blocks extend in the first and second rows, respectively.
3. (Original) The memory device of Claim 2, wherein said sense amplifier array further comprises an alternating zig-zag layout sequence of first and second N-type (or P-type) sense amplifier blocks that extends back-and-forth between the first and second rows.
4. (Original) The memory device of Claim 3, wherein the first row of said sense amplifier array has a first alternating sequence of first column select I/O blocks and first N-type (or P-type) sense amplifier blocks therein; and wherein the second row of said sense amplifier array has a second alternating sequence of second column select I/O blocks and second N-type (or P-type) sense amplifier blocks therein.

5. (Original) The memory device of Claim 4, wherein the first column select I/O blocks in the first alternating sequence are grouped in pairs; and wherein the second column select I/O blocks in the second alternating sequence are grouped in pairs.

6. (Original) The memory device of Claim 5, wherein the first N-type (or P-type) sense amplifier blocks in the first alternating sequence are grouped in pairs; and wherein the second N-type (or P-type) sense amplifier blocks in the second alternating sequence are grouped in pairs.

7. (Original) The memory device of Claim 4, further comprising:

a first column select line that extends between a first column select I/O block and a first N-type (or P-type) sense amplifier block in the first row and between a second column select I/O block and a second N-type (or P-type) sense amplifier block in the second row; and

a first column select line extension that is electrically connected to said first column select line and extends between the first and second rows.

8. (Original) The memory device of Claim 7, wherein said first column select line and said first column select line extension extend in orthogonal directions.

9. (Currently amended) An integrated circuit memory device, comprising:
first and second memory blocks; and

a sense amplifier array that is electrically coupled to said first and second memory blocks by first and second pluralities of pairs of bit lines, respectively, said sense amplifier array having alternating zig-zag layout sequence of first and second column select I/O blocks therein that extends back-and-forth between first and second immediately adjacent rows of said sense amplifier array, which are not separated by memory cells within said first and second memory blocks.

10. (Original) The memory device of Claim 9, wherein each of the first and second column select I/O blocks is electrically coupled by a respective pair of sense bit lines to a respective N-type sense amplifier block and/or P-type sense amplifier block.

11. (Original) The memory device of Claim 9, wherein said sense amplifier array comprises:

a first plurality of isolation blocks that are electrically coupled to first ends of a plurality of pairs of sense bit lines and to the first plurality of pairs of bit lines; and

a second plurality of isolation blocks that are electrically coupled to second ends of the plurality of pairs of sense bit lines and to the second plurality of pairs of bit lines.

12. (Original) The memory device of Claim 9, wherein the first column select I/O blocks are arranged in pairs; and wherein the second column select I/O blocks are arranged in pairs.

13. (Currently amended) An integrated circuit memory device, comprising:

a first column-to-I/O control block comprising a first pair of sense bit lines **[[that are]]** electrically coupled to a first column select I/O block and a first N-type (P-type) sense amplifier block; and

a second column-to-I/O control block immediately adjacent said first column-to-I/O control block, said second column-to-I/O control block comprising a second pair of sense bit lines **[[that are]]** electrically coupled to a second column select I/O block, which extends opposite the first N-type (P-type) sense amplifier block, and a second N-type (P-type) sense amplifier block, which extends opposite the first column select I/O block.

14. (Original) The memory device of Claim 13, further comprising:

a column select line extension that is electrically connected to the first and second column select I/O blocks, said column select line extension extending between the second column select I/O block and the second N-type (P-type) sense amplifier block and also between the first column select I/O block and the first N-type (P-type) sense amplifier block.

15. (Original) An integrated circuit memory device, comprising:

a sense amplifier array having a criss-cross arrangement of column select I/O blocks and sense amplifier blocks therein that collectively form a unit cell layout structure having first and third quadrants that contain first and second column select I/O blocks, respectively, and second and fourth quadrants that contain first and second sense amplifier blocks, respectively.

16. (Original) The memory device of Claim 15, wherein the first column select I/O block comprises a first pair of transistors that are configured to electrically connect a first pair of sense bit lines to a first pair of I/O lines in response to a first column select signal; and wherein the second column select I/O block comprises a second pair of transistors that are configured to electrically connect a second pair of sense bit lines to a second pair of I/O lines in response to the first column select signal.

17. (Currently amended) An integrated circuit memory device, comprising:

a sense amplifier array having a zig-zag layout arrangement of column select I/O blocks therein that span first and second immediately adjacent rows of the sense amplifier array; and

first and second memory blocks that are electrically connected to first and second opposite sides of said sense amplifier array, respectively.

18. (Original) The memory device of Claim 17, wherein a layout of four adjacent column select I/O blocks in said sense amplifier array comprises eight column selection transistors; and wherein gate terminals of the eight column selection transistors are electrically connected together by a common polysilicon gate line.

19. (Original) An integrated circuit memory device, comprising:
a zig-zag layout arrangement of four column select I/O blocks within a sense amplifier array, said four column select I/O blocks comprising eight column selection transistors having gate terminals that are electrically connected together by a common polysilicon gate line.

20. (Original) The memory device of Claim 19, further comprising a column select signal line that is electrically connected to the common polysilicon gate line.